This week I mainly learn the uart bus protocol. It mainly consists of 5 modules. I managed to simulate the function of three modules including uart\_baud\_clkgen, uart\_txd and uart\_txd\_if with three simple testbench listed in the column. At the same time, I begin to learn to use the NCSim software. These simulations were finished on the tool. So far, I still have little thought about how to implement the simulation of the entire 5 modules. Next week, I want to complete the remaining 2 modules and learn to improve the quality of testbench. If possible, I want to learn the FIFO module, because I meet the problem in the uart\_txd\_if. But I can’t understand it. I only treat it as a black box in the simulation process in this work. Thank you for reading.